ELECTRONIC INFORMATION DISCLOSURE STATEMENT

Electronic Version v18

Stylesheet Version v18.0

FILED 6-30-03

Title of Invention	METHODOLOGY FOR FIXING Qcrit AT DESIGN TIMING IMPACT

Application Number : 10/604179

Confirmation Number:

First Named Applicant: Kerry Bernstein

Attorney Docket Number: BUR920010207US1

Art Unit: 2825

Examiner: LIN, SUN JAMES

Search string: (6304998 or 6304998 or 6304998 or 6304998 or 6304998 or 6304998 or 6304998 or 6304998 or 6304998 or 6304998 or 6304998 or 6304998).pn

US Patent Documents

Note: Applicant is not required to submit a paper copy of cited US Patent Documents

init	Cite.No.	Patent No.	Date	Patentee	Kind	Class	Subclass
gg	1	6304998	2001-10- 16	Kamiya, et al	—	716	4
	2	6253352	2001-06- 26	Hanriat, et al	—	716	4
	3	6249901	2001-06- 19	Yuan, et al	—	716	5
	4	6204516	2001-03- 20	Shabde, et al	—	257	48
	5	6090152	2000-07- 18	Hayes, et al	—	716	6
	6	6041169	2000-03- 21	Brennan	—	716	6
	7	5982691	1999-11- 09	Shabde, et al	—	365	206
	8	5974247	1999-10- 26	Yonezawa	—	716	6
	9	5936867	1999-08- 10	Ashuri	—	716	6
	10	5850145	1998-12- 15	Burroughs, et al	—	324	751
	11	5787008	1998-07- 28	Pullela, et al	—	716	6
	12	5400270	1995-03- 21	Fukui, et al	—	716	6
gg	13	5396169	1995-03- 07	Buehler, et all	—	324	158.1

Signature

Examiner Name	Date
James Sun Lin	9-10-04

INFORMATION DISCLOSURE CITATION

(Use several sheets if necessary)

Docket Number (Optional)	Application Number
BUR920010207US1 (15821)	10/604179
Applicant(s)	
Kerry Bernstein, et al.	
Filing Date	**Group Art Unit**
6-25-03	2825 Unassigned

U.S. PATENT DOCUMENTS

*EXAMINER INITIAL	REF	DOCUMENT NUMBER	DATE	NAME	CLASS	SUBCLASS	FILING DATE IF APPROPRIATE

FOREIGN PATENT DOCUMENTS

	REF	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUBCLASS	Translation YES	Translation NO

OTHER DOCUMENTS *(Including Author, Title, Date, Pertinent Pages, Etc.)*

PSL		Chan, "Technique for Reducing Personalized Array Soft Errors', RESEARCH DISCLOSURE, Kenneth Mason Publications Ltd, England, October 1989, No. 306
PSL		Jarvela, et al., "MLC DESIGN TO LIMIT SOFT ERROR FAILS", IBM Technical Disclosure Bulletin, Vol. 27, No. 2, July 1984, pp. 1343-1344

EXAMINER	DATE CONSIDERED
James Jun Liu	9-10-04

EXAMINER: Initial if citation considered, whether or not citation is in conformance with MPEP Section 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

INFORMATION DISCLOSURE CITATION

(Use several sheets if necessary)

Docket Number (Optional)	Application Number
BUR920010207US1 (15821)	10/604179 Unassigned
Applicant(s) Kerry Bernstein, et al.	
Filing Date 6-30-04 Herewith	**Group Art Unit** 2825 ~~Unassigned~~

U.S. PATENT DOCUMENTS

*EXAMINER INITIAL	REF	DOCUMENT NUMBER	DATE	NAME	CLASS	SUBCLASS	FILING DATE IF APPROPRIATE

FOREIGN PATENT DOCUMENTS

	REF	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUBCLASS	Translation YES	Translation NO

OTHER DOCUMENTS *(Including Author, Title, Date, Pertinent Pages, Etc.)*

JSR		Geppert, et al., "CMOS DRAM DESIGN LAYOUT TO IMPROVE SOFT ERROR IMMUNITY", IBM Technical Disclosure Bulletin, Vol. 34, No. 4B, September 1991, pp. 27-28
JSR		Dai, et al., "Alpha-SER Modeling & Simulation for Sub-0.25μm CMOS Technology", 1999 Symposium on VLSI Technology Digest of Technical Papers, pp. 81-82

EXAMINER	DATE CONSIDERED
James Dun Fitz	9-10-04

EXAMINER: Initial if citation considered, whether or not citation is in conformance with MPEP Section 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.